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Asynchronous Design for Parallel Processing Architectures

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Goal: The objective of this research is to provide an interconnect synthesis methodology which facilitates a modular design approach without compromising the global performance. The main tasks of this effort will be the development of the theory for optimal interconnect circuit synthesis from a high-level specification, with emphasis on testability and fault-tolerance asynchronous interface among concurrently computing hardware, and the application of this design methodology to physical implementations of parallel processing systems.

Progress:

In the past six months, our major research effort has been directed toward the testability of asynchronous circuits. Testability has become a major design consideration in IC industry and the question that whether asynchronous circuits would simplify the testing tasks is to be answered. Asynchronous combinational circuits had been shown to be fully testable with single-stuck-at-faults (SSAFs) if precharged circuits were used for implementation; however, the testability of asynchronous control circuits (sequential circuits with environmental constraints) had not been addressed. Level-sensitive scan-path design can be used to aid testing in asynchronous sequential circuits, but scan-path design usually requires too long a testing delay. We are most interested in incorporating testability directly into circuit synthesis.

We considered the problem of testability for two areas of asynchronous design: speed-independent circuits and self-timed circuits. Speed-independent circuits are designed to work independently of the gate delays in the circuits. Self-timed circuits are designed to work assuming that each gate follows a minimum and maximum delay assumption. Both kinds of circuits under the different delay assumptions can be designed to be hazard-free through a synthesis procedure.

We used the property of semi-modularity to show that stuck-at-faults (SAF) are fully testable in a hazard-free speed-independent circuit. Semi-modularity defines that if a transition in a circuit is enabled, then the transition must be fired before it is disabled. We proved that this property is a necessary property of a speed-independent hazard-free circuit by construction. We also proved that the same semi-modularity property is a sufficient condition for a circuit to be self-diagnostic; that is, the circuit will halt itself in response to any SAFs [1]. This important theoretical result states that for speed-independent circuits, designing for testability is no more difficult than designing for hazard-freedom. We have developed a CAD program which accepts a circuits implementation and determines if the circuit is semi-modular, and hence if the circuit is self-diagnostic to SAFs.

We continued our research on self-timed circuit testability, under the assumption that the circuit is hazard-free if each gate follows a set of predetermined minimum and maximum gate delays. We constructed a general model for asynchronous control circuits, decomposing them into a next-state block, a C-element array, and an output-logic block. A comprehensive study of testing such circuits has been conducted and the sufficient conditions under which a given circuit can be ensured to be fully testable to SSAFs have been constructed. Our conditions do not require direct access to the C-element array and incur no added circuitry [2]. We have developed a CAD tool which excepts as input a gate-level description of the circuit implementation with minimum and maximum gate delays and determines if the circuit is fully SSAF testable using the sufficient conditions derived in [2]. If the circuit is not fully testable, the tool alerts the user of the nodes and the associated SAF. We are currently investigating necessary conditions for SAF testability to guide the synthesis procedure so that fully testable asynchronous control circuits can be synthesized from a high-level description.

Future research for the next two quarters:

In the next two quarters, in addition to continuing our work on the synthesis of *timed* asynchronous circuits (please refer to the research summary of June 1990), we plan to develop means of converting a hazardous implementation (implementation with logic hazards) to a hazard-free implementation given that the circuit does not possess any function hazards. It has been shown that with the inclusion of arbitrary delay elements it is possible to create a hazard-free self-timed design from high-level descriptions. We propose to investigate the synthesis of minimal hazard-free circuits *without* added delay elements, because such elements are bound to degrade circuit performance. This is a difficult problem, as we need first to prove that such an implementation exist and then to construct a generic algorithm that will generate the corresponding gate-level description.

With the understanding of synthesis of timed asynchronous circuit, we plan to combine both the synthesis and testability of asynchronous circuits into a common paradigm. Different fault models will be investigated to address timing issues in testing asynchronous circuits and to facilitate automatic synthesis of fully testable asynchronous circuits.

References

[1]. Peter A. Beerel and Teresa H.-Y. Meng, "Semi-Modularity and Self-Diagnostic Asynchronous Control Circuits", to be published in *Advanced Research in VLSI*, MIT Press, March 1991, and to be presented in the *Workshop of High-Level Synthesis*, March 1991.

[2]. Peter A. Beerel and Teresa H.-Y. Meng. "Testability of Asynchronous Self-Timed Control Circuits with Delay Assumptions", submitted to *28th ACM/IEEE Design Automation Conference*, November, 1990.